Amendments to the Claims:

CLAIMS:

1. (Currently Amended) A method for transmitting a "J" bit block of data from a first electronic unit to a second electronic unit over a signaling bus having "K" signaling conductors, where zero to "K-1" of the signaling conductors is faulty, the method comprising the steps of:

identifying faulty and nonfaulty signaling conductors in the signaling bus;

setting a fault status of the signaling conductors in the first electronic unit and in the second electronic unit, using information found by the step of identifying faulty and nonfaulty signaling conductors in the signaling bus;

determining "F", the number of faulty signaling conductors in the signaling bus;

determining "K-F", the number of nonfaulty signaling conductors in the signaling bus; and

transmitting the "J" bit block of data over the "K-F" nonfaulty signaling conductors using "J/(K-F)" beats, plus an additional beat if a remainder exists;

the step of transmitting further comprises the steps of:

selecting a "K" bit group of data from the "J" bit block of data;

transmitting, on a beat, "K-F" bits of the "K" bit group of data, using the "K-F" nonfaulty conductors;

storing the "F" bits in the "K" bit group that cannot be transmitted, on the beat, due to the "F" faulty conductors in the signaling bus;

repeating the above three steps until all "J" bits of the "J" bit block of data have been selected; and

transmitting the stored "F" bits on one or more additional beats, using one or more of the "K-F" nonfaulty signaling conductors;

the step of storing the "F" bits further comprising the step of shifting at least one bit of the "F" bits into a first end of a shift register; and

transmitting at least one of the bits of the shift register to a nonfaulty signaling conductor.

2. (Cancelled)
3. (Cancelled)
4. (Cancelled)
5. (Currently Amended) The method of claim [[4]] 1, further comprising the step of moving a particular bit in the shift register to align that particular bit for coupling to a nonfaulty signaling conductor.
6. (Currently Amended) The method of claim [[2]] 1, further comprising the steps of:
   storing, in the second electronic unit, "K-F" bits per beat for "J/(K-F)" beats; and storing remainder bits in an additional beat, if "J/(K-F)" results in a remainder.
7. (Original) The method of claim 1, further comprising the steps of:
   selecting a "K-F" bit group of bits from the "J" bit block of data on the first electronic unit;
   transmitting the "K-F" bit group of bits from the first electronic unit to the second electronic unit using the "K-F" nonfaulty signaling conductors in the signaling bus, using a beat of the signaling bus;
   repeating the previous steps until all "K-F" bit groups have been transmitted; and
   transmitting any remaining bits of the "J" bit block of data on the first electronic unit to the second electronic unit using some or all of the "K-F" nonfaulty signaling conductors, using an additional beat of the signaling bus.

8. (Currently Amended) An apparatus for transmitting a "J" bit block of data from a first electronic unit to a second electronic unit comprising:

a first block of data in the first electronic unit holding "J" bits for transmission;

storage in the second electronic capable of holding a second block of data having "J" bits;

a signaling bus having "K" signaling conductors coupling the first electronic unit to the second electronic unit, "K" greater than one, the signaling bus having [["F"]] one (1) faulty signaling conductors and "K-[[F]] 1" nonfaulty signaling conductors;

a diagnostic unit coupled to the first electronic unit and to the second electronic unit capable of identifying the "[[F]] 1" faulty signaling conductors and the "K-[[F]] 1" nonfaulty signaling conductors on the signaling bus and storing fault identification information in the first electronic unit and in the second electronic unit; [[and]]

a driving sequencer in the first electronic unit that, respondent to the fault identification information, transmits the "J" bits of data using "J/(K-[[F]] 1)" beats, plus an additional beat if a remainder exists, using only the "K-[[F]] 1" nonfaulty conductors;

a shift register having "K" bits, configured to receive, during each beat, at a first end of the shift register, a bit directed to the faulty signaling conductor, the shift register, when full, configured to be rotated for a first rotation, during which first rotation, a bit at a second end of the shift register is received at the first end of the shift register;

the apparatus configured to, following the first rotation, transmit K-1 bits of the shift register onto the nonfaulty signaling conductors;

the shift register further configured to be rotated for a second rotation, during which second rotation, a bit at the second end of the shift register is received at the first end of the shift register;

the apparatus configured to, following the second rotation, transmit the remaining untransmitted bit of the "J" bits on a nonfaulty signaling conductor.

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)